Remarks

Claims 4 and 5 are presently pending and stand rejected. Claims 1-3 and 6-11 are cancelled without prejudice. Claim 4 is amended.

Claim 4 was rejected under 35 U.S.C. § 101. Examiner has indicated that claim 4 does not produce a "useful or tangible result" and that "the claimed invention is used for verifying unspecified condition of a system".

Assignee respectfully traverses the rejection. It is noted that in claim 4, "verify the first system" and "verify the second system" are tangible and produces a result that has real world value because the "first circuitry" is physically configured to "realize" the "first system" and the "second circuitry" is physically configured to "realize" the "second system".

Examiner has maintained the rejection indicating that:

"The claims as a while are directed to verifying a system which the final steps is also verifying a system and therefore no tangible results, and thus no practical application is produced."

Once again, Assignee submits that "verifying the first system" and "verifying the second system" are a tangible results and a practical application is produced. Additionally, claim 12 is added reciting "wherein verifying the plurality of systems further comprises detecting errors in the plurality of systems". Clearly "detecting errors" is a tangible result.

Claim 4 was also rejected under 35 U.S.C. § 102(f) on the grounds that "applicant did not invent the claimed subject matter". Examiner has indicated that the "have not shown how the emulator is transformed in their claimed invention to overcome the rejection. However, this transformation is well known for many chip makers that use a hardware emulator as follows. [Quoting Specification paragraph 0006]".

Assignee respectfully traverses the rejection and submits that the foregoing Specification 0006 does not teach "a second circuitry configured to realize and verify the second system on another chip *while the first circuit verifies the first system on chip*, the second circuitry directly connected to the first circuitry". Clearly, by configuring the second circuitry to "realize and verify the

second system on another chip *while the first circuit verifies the first system on chip"*, a transformation of the emulator occurs.

Claim 4 was also rejected under 35 U.S.C. § 102(e) as being anticipated by Rohlfleisch. Examiner has made citation to Rohlfleisch [0039]. However, Rohlfeisch [0039] states that "Advantageously, the emulator circuits 104, 108 and the emulator interface circuit 110 permit an SOC designer or programmer to test, evaluate, and/or debug the processor core 102 and/or the other core 106 using the emulation interface circuit 110." Note, however that "emulator circuits 104, 108" are in fact, two emulator circuits. In contrast, Assignee claims "a hardware emulator for verifying a first system on a chip and a second system on another chip" – noting the use of the singular context in the claim.

Additionally, Rohlfleisch also does not teach "a hardware emulator for verifying a first system on a chip and a second system on another chip, said hardware emulator comprising: a first circuitry configured to realize and verify the first system on a chip, said first circuitry further comprising at least one output port for providing verification results from the first circuitry; and a second circuitry configured to realize and verify the second system on another chip while the first circuit verifies the first system on chip, the second circuitry directly connected to the first circuitry." As noted above, "the emulator circuits 104, 108 and the emulator interface circuit 110 permit an SOC designer or programmer to test, evaluate, and/or debug the processor core 102 and/or the other core 106". Clearly, emulator circuit 104 and emulator circuit 108 are not directly connected.

For convenience, Rohlfleisch, Figure 1 is shown below.

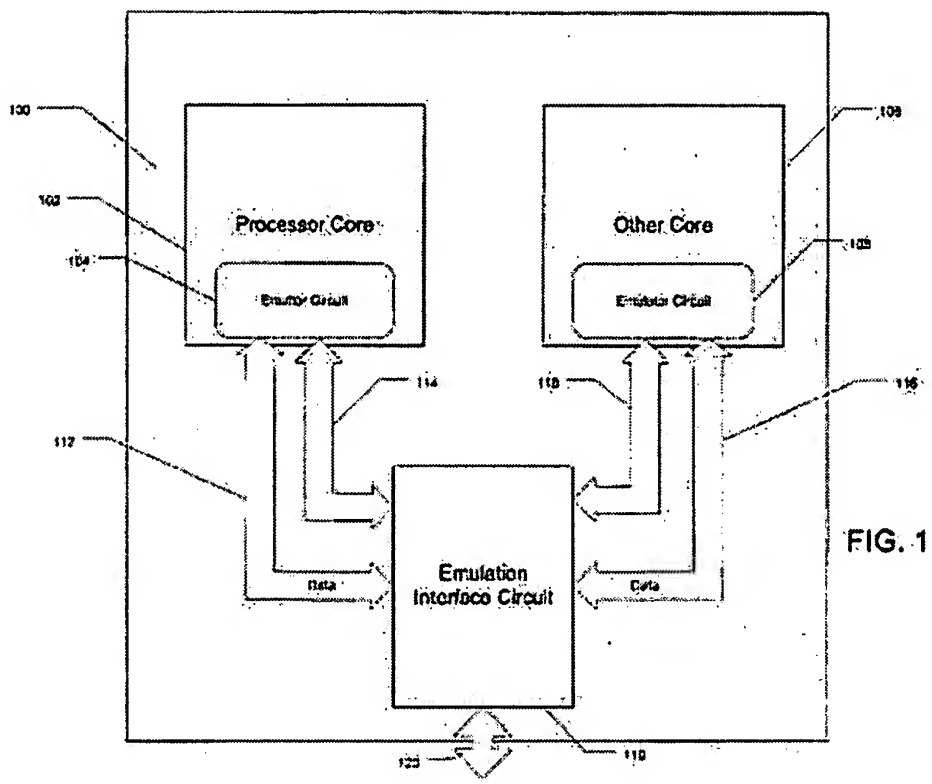


FIG. 1

Rohlfleisch, Figure 1.

Accordingly, Assignee respectfully requests that Examiner withdraw the rejection to claims 4, 5, and 12.

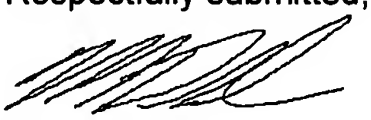
Additionally, Figures 4 and 5 have been objected. Assignee hereby provides Examiner with replacement drawings.

Conclusion

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Date: April, 29, 2009

Respectfully submitted,



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